

MCR69-2, MCR69-3

Silicon Controlled Rectifiers Reverse Blocking Thyristors

Designed for overvoltage protection in crowbar circuits.

Features

- Glass-Passivated Junctions for Greater Parameter Stability and Reliability
- Center-Gate Geometry for Uniform Current Spreading Enabling High Discharge Current
- Small Rugged, Thermowatt Package Constructed for Low Thermal Resistance and Maximum Power Dissipation and Durability
- High Capacitor Discharge Current, 750 Amps
- Pb-Free Packages are Available*

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) ($T_J = -40$ to $+125^\circ\text{C}$, Gate Open) MCR69-2 MCR69-3	V_{DRM} , V_{RRM}	50 100	V
Peak Discharge Current (Note 2)	I_{TM}	750	A
On-State RMS Current (180° Conduction Angles; $T_C = 85^\circ\text{C}$)	$I_{T(RMS)}$	25	A
Average On-State Current (180° Conduction Angles; $T_C = 85^\circ\text{C}$)	$I_{T(AV)}$	16	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, $T_J = 125^\circ\text{C}$)	I_{TSM}	300	A
Circuit Fusing Considerations ($t = 8.3$ ms)	I^2t	375	A^2s
Forward Peak Gate Current ($t \leq 1.0$ μs , $T_C = 85^\circ\text{C}$)	I_{GM}	2.0	A
Forward Peak Gate Power ($t \leq 1.0$ μs , $T_C = 85^\circ\text{C}$)	P_{GM}	20	W
Forward Average Gate Power ($t = 8.3$ ms, $T_C = 85^\circ\text{C}$)	$P_{G(AV)}$	0.5	W
Operating Junction Temperature Range	T_J	-40 to $+125$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to $+150$	$^\circ\text{C}$
Mounting Torque	–	8.0	in. lb.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.
2. Ratings apply for $t_w = 1$ ms. See Figure 1 for I_{TM} capability for various duration of an exponentially decaying current waveform, t_w is defined as 5 time constants of an exponentially decaying current pulse.
3. Test Conditions: $I_G = 150$ mA, $V_D = \text{Rated } V_{DRM}$, $I_{TM} = \text{Rated Value}$, $T_J = 125^\circ\text{C}$.

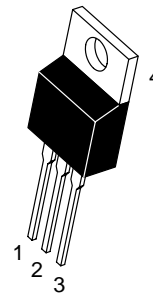
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

<http://onsemi.com>

SCRs
25 AMPERES RMS
50 thru 100 VOLTS



MARKING DIAGRAM



TO-220AB
CASE 221A
STYLE 3

A = Assembly Location
Y = Year
WW = Work Week
MCR69 = Device Code
x = 2 or 3
AKA = Location Code

PIN ASSIGNMENT

Pin	Assignment
1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

Device	Package	Shipping†
MCR69-2	TO220AB	500/Box
MCR69-2G	TO220AB (Pb-Free)	500/Box
MCR69-3	TO220AB	500/Box
MCR69-3G	TO220AB (Pb-Free)	500/Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.5	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	60	$^{\circ}\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes 1/8 in from Case for 10 Seconds	T_L	260	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current ($V_{AK} = \text{Rated } V_{DRM} \text{ or } V_{RRM}, \text{ Gate Open}$)	I_{DRM}, I_{RRM}	–	–	10	μA
$T_J = 25^{\circ}\text{C}$		–	–	2.0	mA
$T_J = 125^{\circ}\text{C}$		–	–		

ON CHARACTERISTICS

Peak Forward On-State Voltage ($I_{TM} = 50 \text{ A}$) (Note 4) ($I_{TM} = 750 \text{ A}, t_w = 1 \text{ ms}$) (Note 5)	V_{TM}	–	–	1.8	V
		–	6.0	–	
Gate Trigger Current (Continuous dc) ($V_D = 12 \text{ V}, R_L = 100 \Omega$)	I_{GT}	2.0	7.0	30	mA
Gate Trigger Voltage (Continuous dc) ($V_D = 12 \text{ V}, R_L = 100 \Omega$)	V_{GT}	–	0.65	1.5	V
Gate Non-Trigger Voltage ($V_D = 12 \text{ Vdc}, R_L = 100 \Omega, T_J = 125^{\circ}\text{C}$)	V_{GD}	0.2	0.40	–	V
Holding Current ($V_D = 12 \text{ V}, \text{ Initiating Current} = 200 \text{ mA}, \text{ Gate Open}$)	I_H	3.0	15	50	mA
Latching Current ($V_D = 12 \text{ Vdc}, I_G = 150 \text{ mA}$)	I_L	–	–	60	mA
Gate Controlled Turn-On Time (Note 6) ($V_D = \text{Rated } V_{DRM}, I_G = 150 \text{ mA}$) ($I_{TM} = 50 \text{ A Peak}$)	t_{gt}	–	1.0	–	μs

DYNAMIC CHARACTERISTICS

Critical Rate-of-Rise of Off-State Voltage ($V_D = \text{Rated } V_{DRM}, \text{ Gate Open}, \text{ Exponential Waveform}, T_J = 125^{\circ}\text{C}$)	dv/dt	10	–	–	$\text{V}/\mu\text{s}$
Critical Rate-of-Rise of On-State Current $I_G = 150 \text{ mA}$	di/dt	–	–	100	$\text{A}/\mu\text{s}$
					$T_J = 125^{\circ}\text{C}$

- Pulse duration $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- Ratings apply for $t_w = 1 \text{ ms}$. See Figure 1 for I_{TM} capability for various durations of an exponentially decaying current waveform. t_w is defined as 5 time constants of an exponentially decaying current pulse.
- The gate controlled turn-on time in a crowbar circuit will be influenced by the circuit inductance.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On State Voltage
I_H	Holding Current

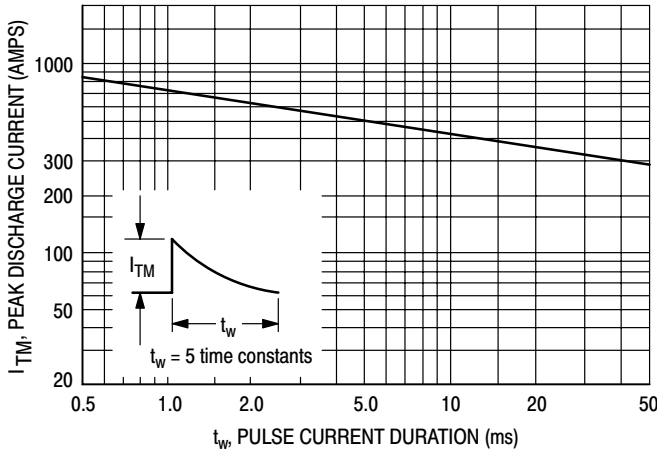
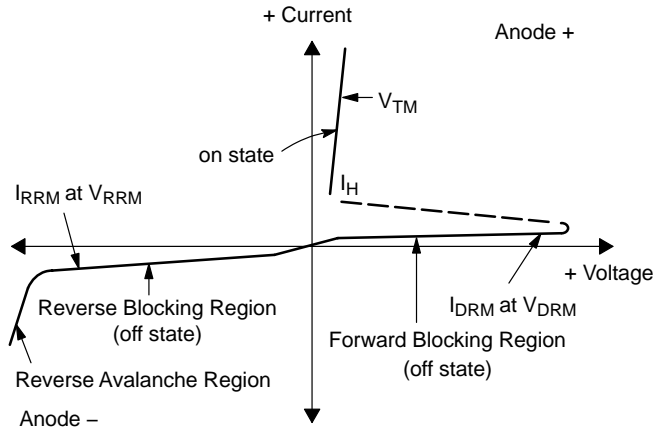


Figure 1. Peak Capacitor Discharge Current

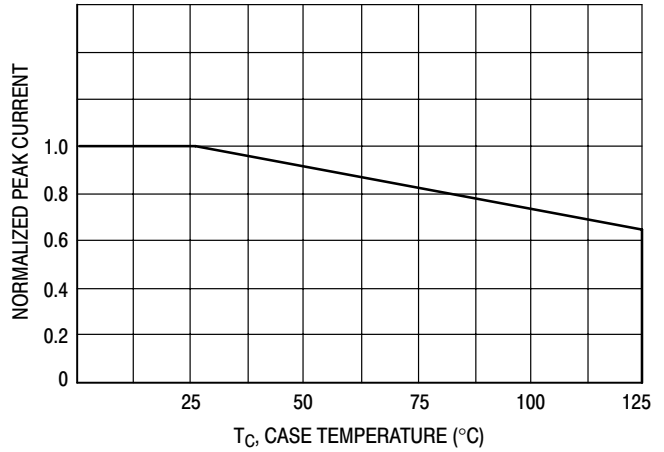


Figure 2. Peak Capacitor Discharge Current Derating

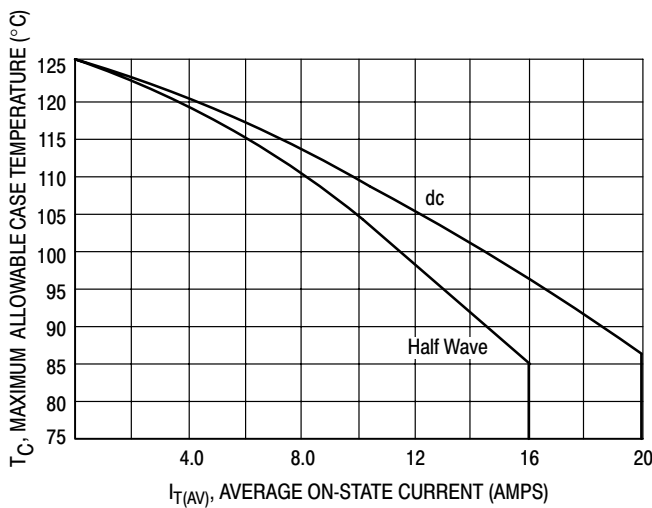


Figure 3. Current Derating

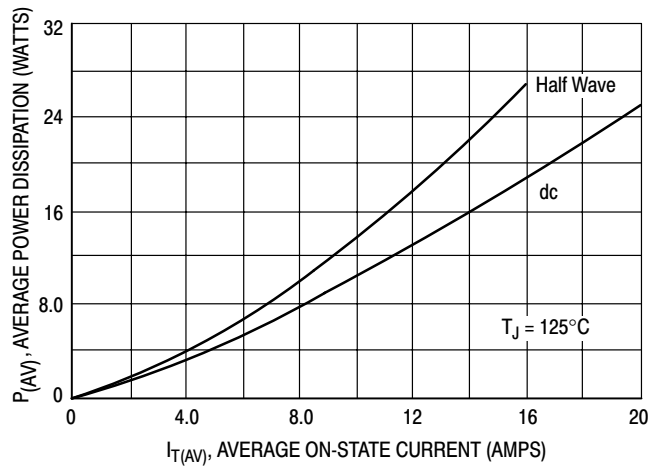


Figure 4. Maximum Power Dissipation

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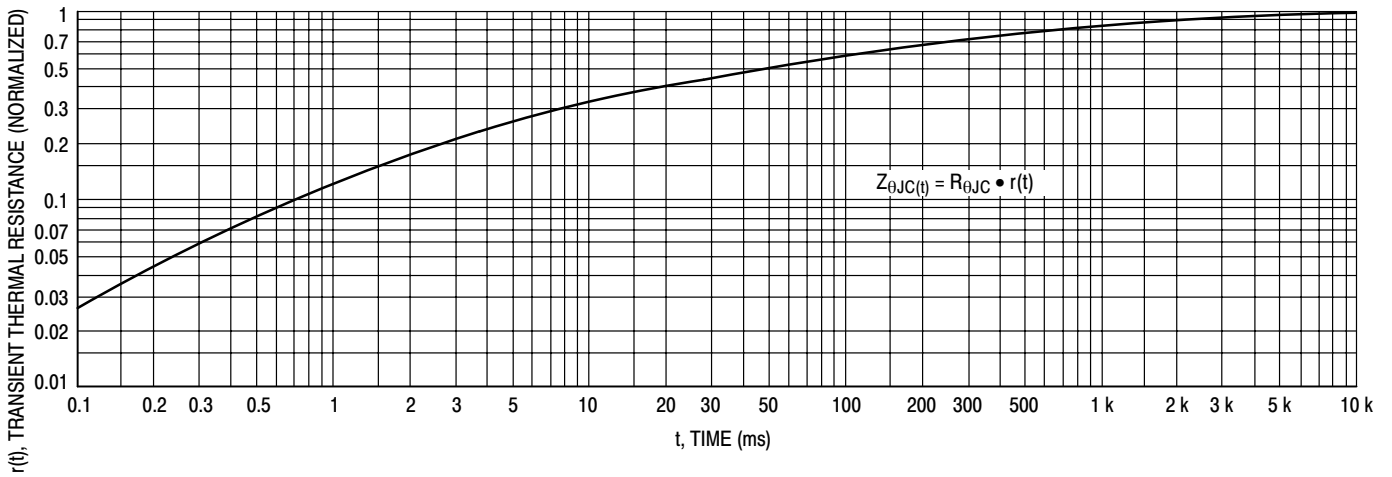


Figure 5. Thermal Response

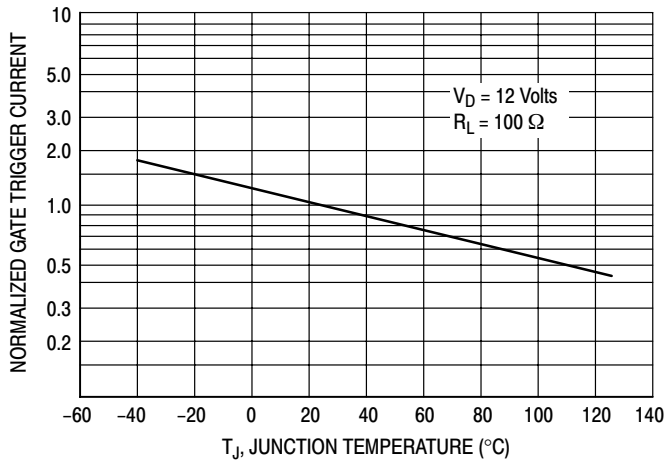


Figure 6. Gate Trigger Current

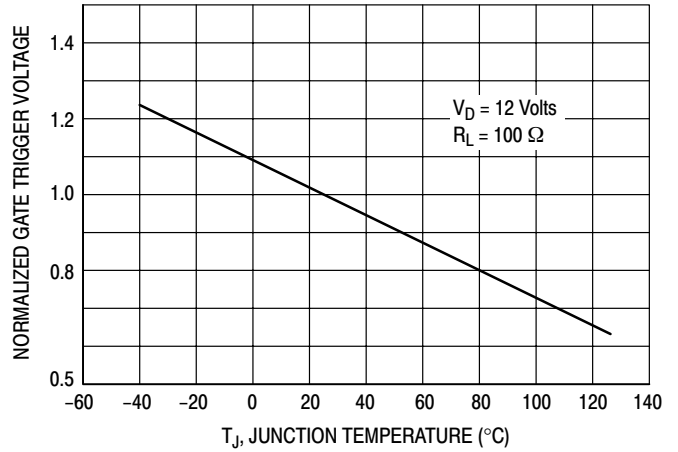


Figure 7. Gate Trigger Voltage

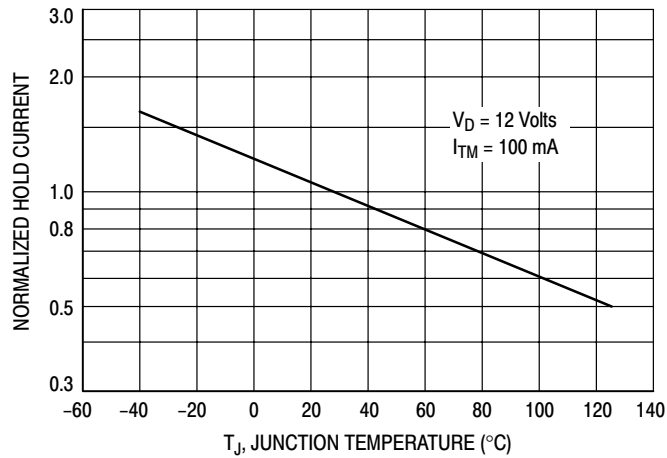
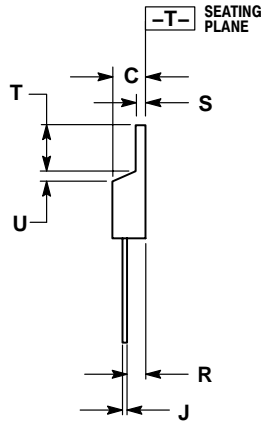
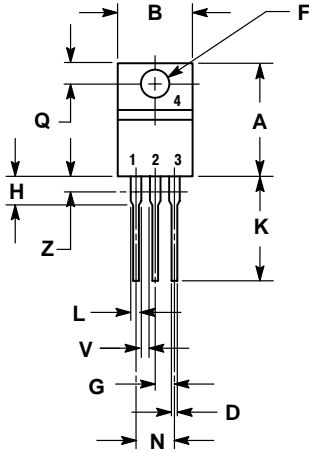


Figure 8. Holding Current

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PACKAGE DIMENSIONS

TO-220AB
CASE 221A-07
ISSUE AA



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 3:
1. CATHODE
 2. ANODE
 3. GATE
 4. ANODE

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